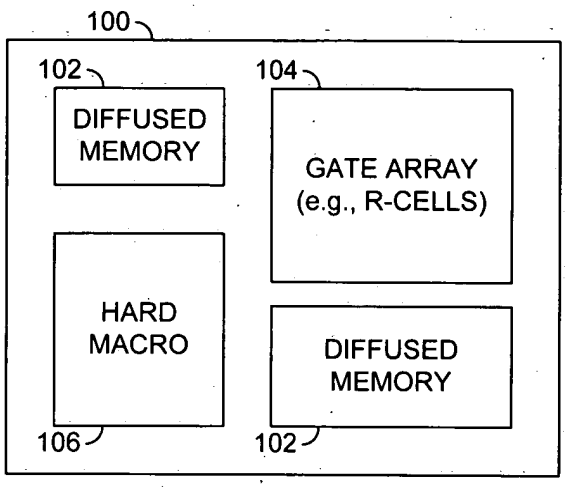
100
102
DIFFUSED MEMORY
104
GATE ARRAY (e.g., R-CELLS)
HARD MACRO
106
DIFFUSED MEMORY
102

FIG. 1

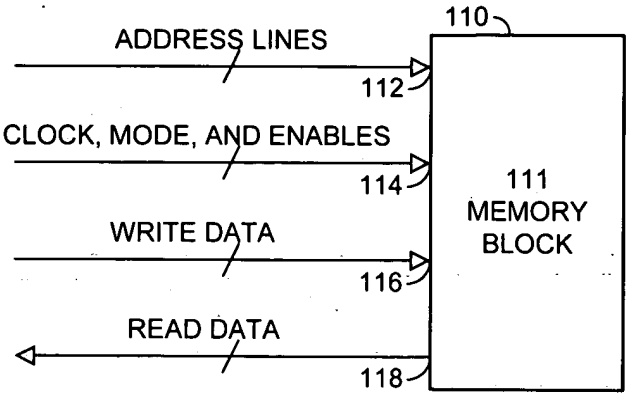
110
ADDRESS LINES
112
CLOCK, MODE, AND ENABLES
114
WRITE DATA
116
READ DATA
118
111
MEMORY
BLOCK

FIG. 2

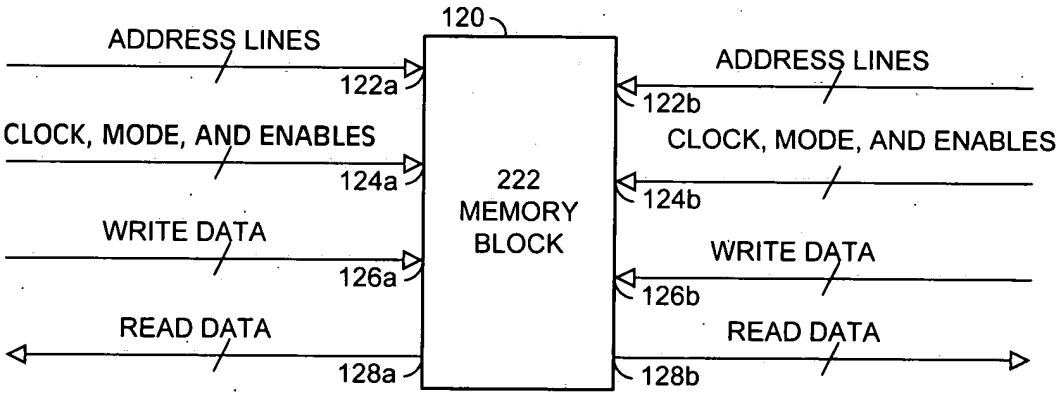
120
ADDRESS LINES
122a
CLOCK, MODE, AND ENABLES
124a
WRITE DATA
126a
READ DATA
128a
222
MEMORY
BLOCK
ADDRESS LINES
122b
CLOCK, MODE, AND ENABLES
124b
WRITE DATA
126b
READ DATA
128b

FIG. 3

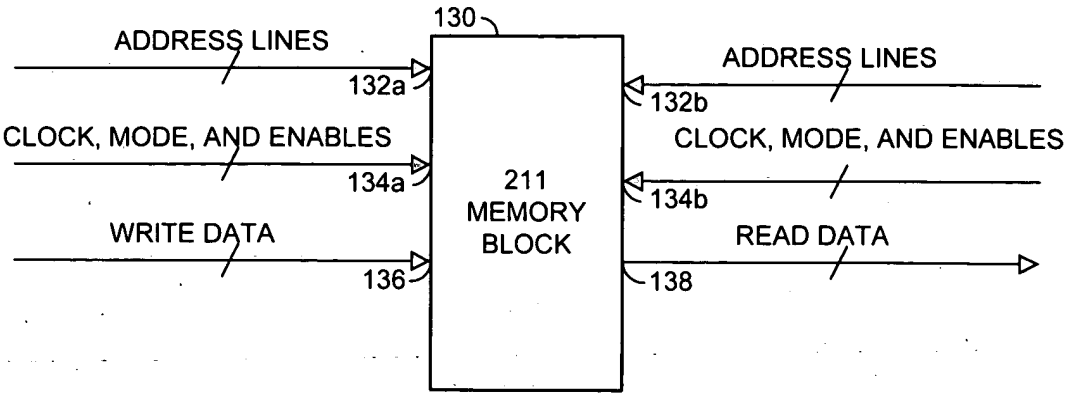
130
ADDRESS LINES
132a
CLOCK, MODE, AND ENABLES
134a
WRITE DATA
136
211
MEMORY
BLOCK
ADDRESS LINES
132b
CLOCK, MODE, AND ENABLES
134b
READ DATA
138

FIG. 4

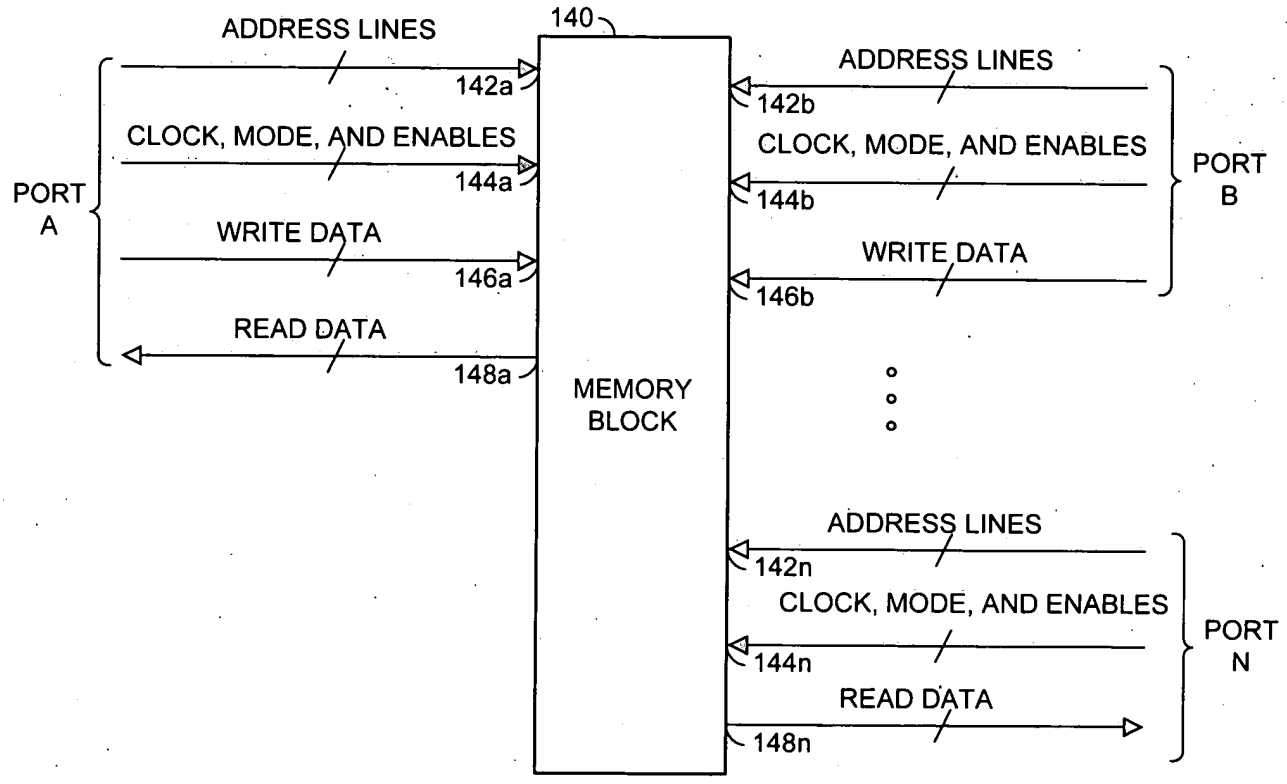
140
ADDRESS LINES
142a
CLOCK, MODE, AND ENABLES
144a
WRITE DATA
146a
READ DATA
148a
PORT
A
MEMORY
BLOCK
ADDRESS LINES
142b
CLOCK, MODE, AND ENABLES
144b
WRITE DATA
146b
PORT
B
ADDRESS LINES
142n
CLOCK, MODE, AND ENABLES
144n
READ DATA
148n
PORT
N

FIG. 5

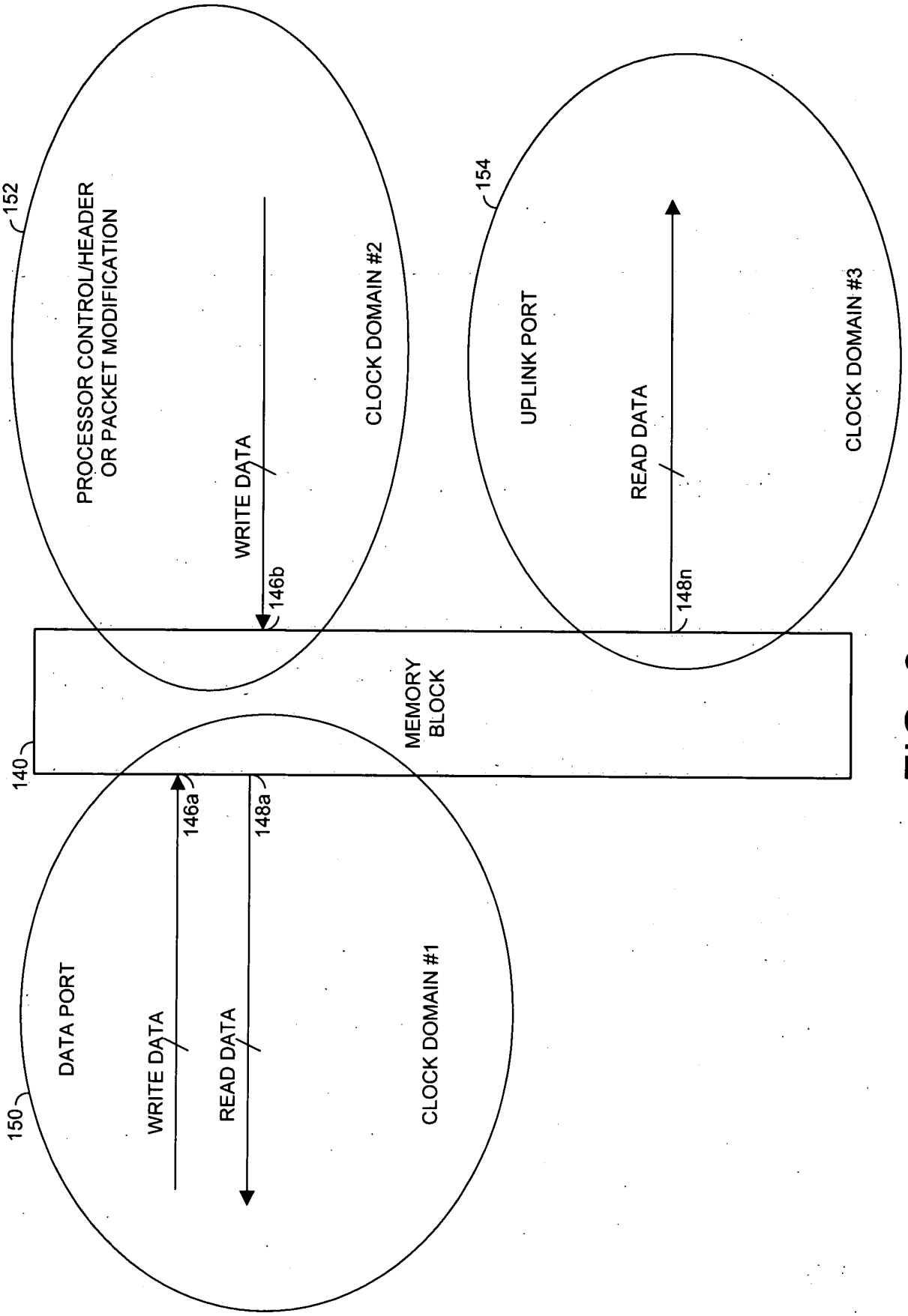
152
PROCESSOR CONTROL/HEADER OR PACKET MODIFICATION
WRITE DATA
146b
CLOCK DOMAIN #2
154
UPLINK PORT
READ DATA
148n
CLOCK DOMAIN #3
140
MEMORY BLOCK
150
DATA PORT
WRITE DATA
146a
READ DATA
148a
CLOCK DOMAIN #1

FIG. 6

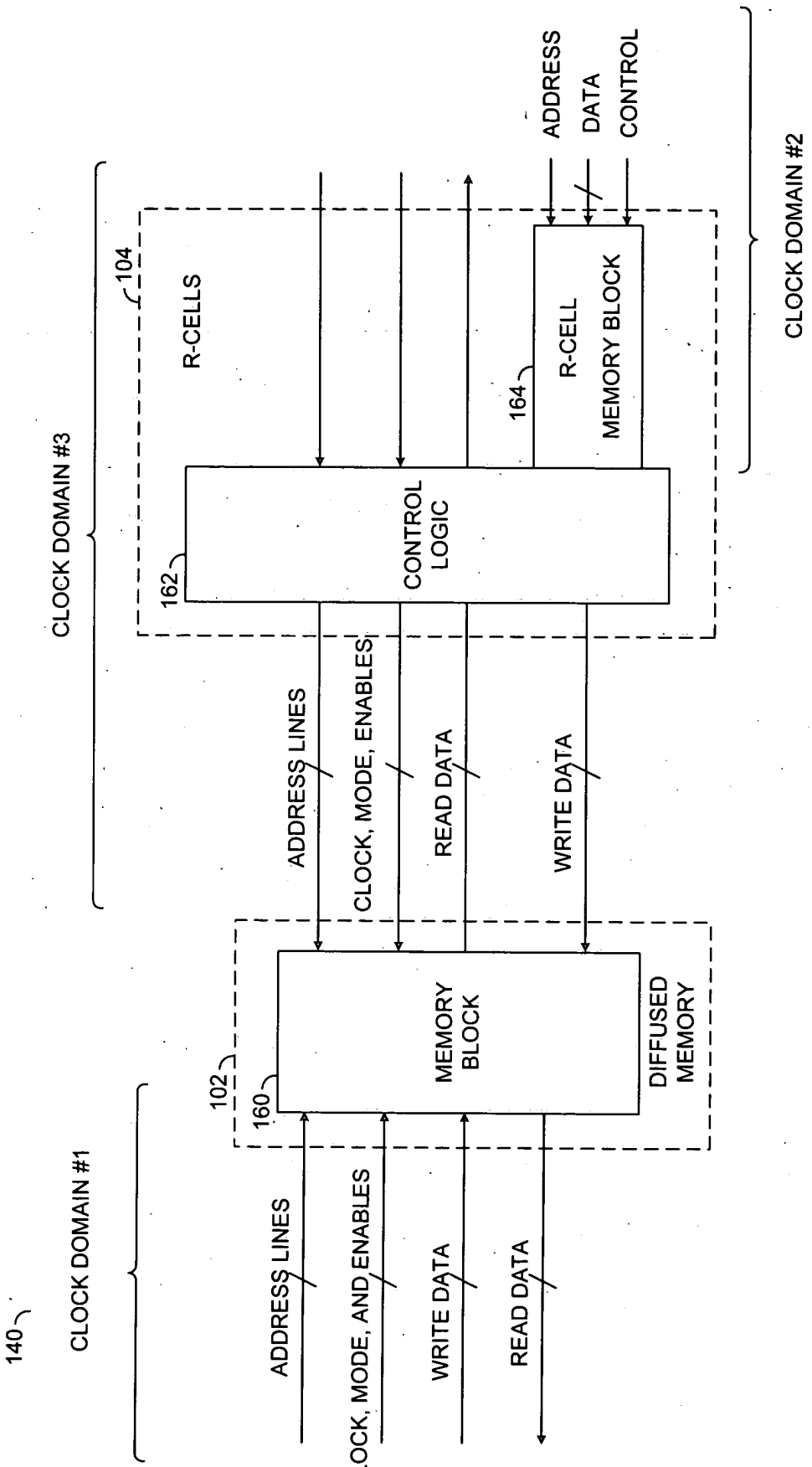
140
CLOCK DOMAIN #1
CLOCK DOMAIN #3
CLOCK DOMAIN #2
102
160
MEMORY BLOCK
DIFFUSED MEMORY
104
R-CELLS
162
CONTROL LOGIC
164
R-CELL MEMORY BLOCK
ADDRESS LINES
CLOCK, MODE, AND ENABLES
WRITE DATA
READ DATA
ADDRESS LINES
CLOCK, MODE, ENABLES
READ DATA
WRITE DATA
ADDRESS
DATA
CONTROL

FIG. 7

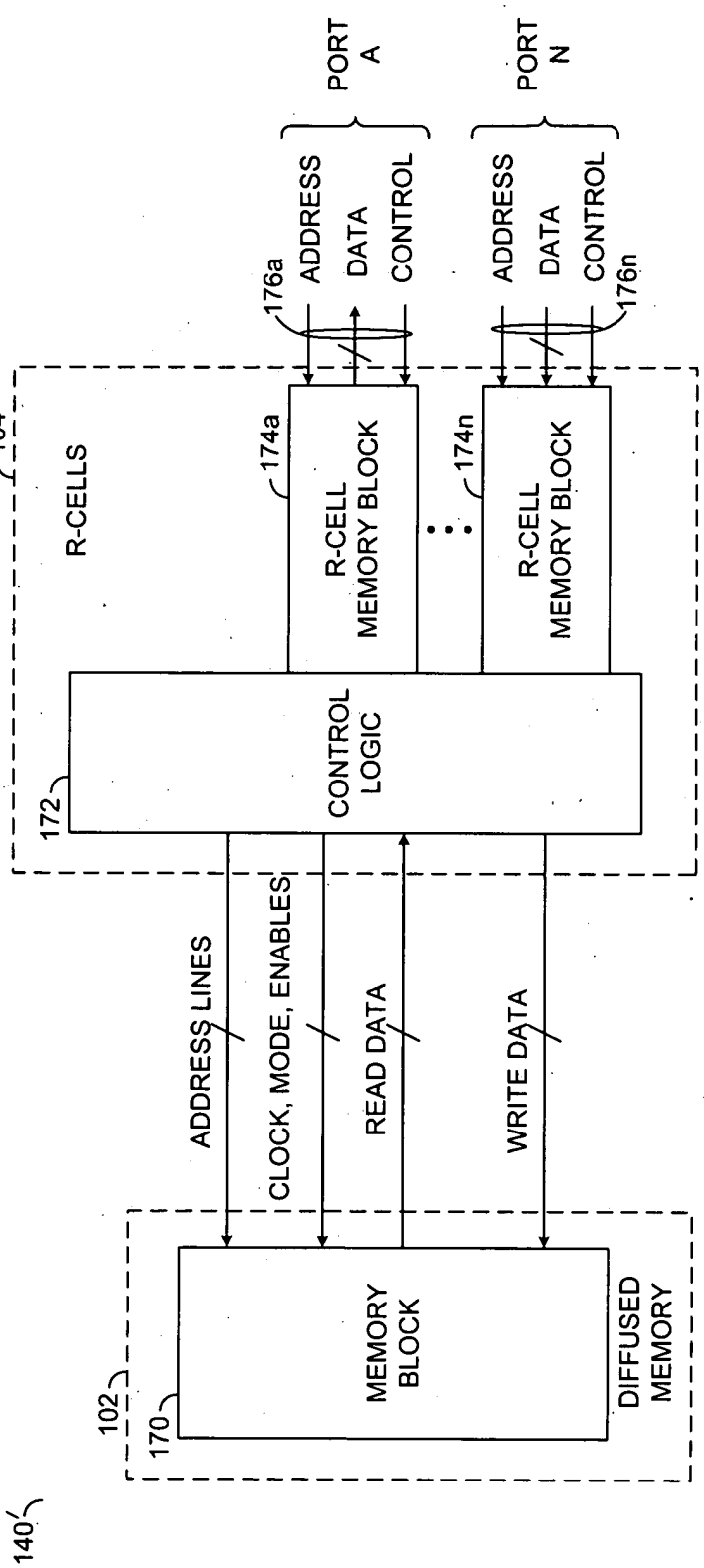
140
102
DIFFUSED MEMORY
170
MEMORY BLOCK
ADDRESS LINES
CLOCK, MODE, ENABLES
READ DATA
WRITE DATA
104
R-CELLS
172
CONTROL LOGIC
174a
R-CELL MEMORY BLOCK
174n
R-CELL MEMORY BLOCK
176a
ADDRESS
DATA
CONTROL
176n
ADDRESS
DATA
CONTROL
PORT A
PORT N

FIG. 8

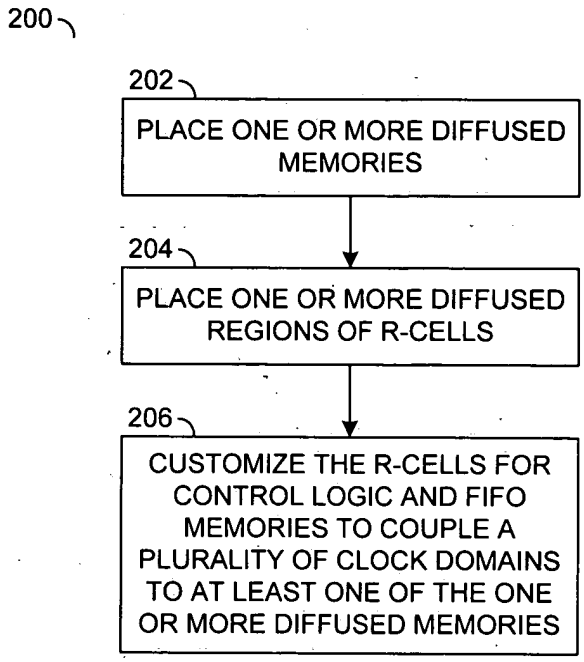
200
202
PLACE ONE OR MORE DIFFUSED MEMORIES
204
PLACE ONE OR MORE DIFFUSED REGIONS OF R-CELLS
206
CUSTOMIZE THE R-CELLS FOR CONTROL LOGIC AND FIFO MEMORIES TO COUPLE A PLURALITY OF CLOCK DOMAINS TO AT LEAST ONE OF THE ONE OR MORE DIFFUSED MEMORIES

FIG. 9

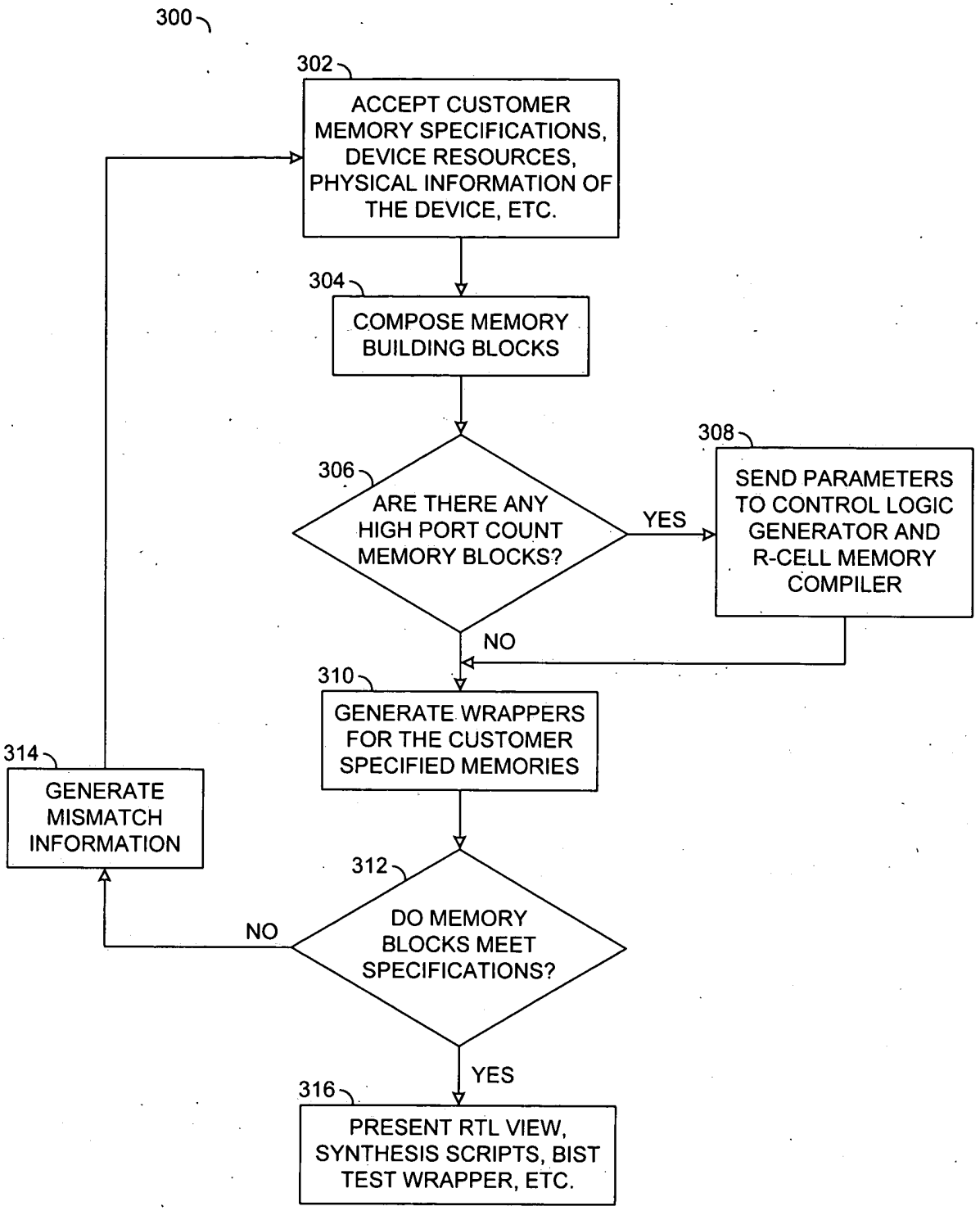
300
302
ACCEPT CUSTOMER MEMORY SPECIFICATIONS, DEVICE RESOURCES, PHYSICAL INFORMATION OF THE DEVICE, ETC.
304
COMPOSE MEMORY BUILDING BLOCKS
306
ARE THERE ANY HIGH PORT COUNT MEMORY BLOCKS?
YES
308
SEND PARAMETERS TO CONTROL LOGIC GENERATOR AND R-CELL MEMORY COMPILER
NO
310
GENERATE WRAPPERS FOR THE CUSTOMER SPECIFIED MEMORIES
312
DO MEMORY BLOCKS MEET SPECIFICATIONS?
NO
314
GENERATE MISMATCH INFORMATION
YES
316
PRESENT RTL VIEW, SYNTHESIS SCRIPTS, BIST TEST WRAPPER, ETC.

FIG. 10